**module HalfAdder (a, b, sum, carry);**

**input a,b;**

**output sum,carry;**

**xor x1 (sum, a, b);**

**and a1 (carry, a, b);**

**endmodule**

**--------------------------------------------------**

**module sum (su, a, b);**

**input a,b;**

**output su;**

**xor x1 (su,a,b);**

**endmodule**

**--------------------------------------------------**

**module carry (a, b, car);**

**input a,b;**

**output car;**

**and a1 (car, a, b);**

**endmodule**

**--------------------------------------------------**

**module HA (i1, i2, S, C);**

**input i1, i2;**

**output S, C;**

**sum s1 (S, i1, i2);**

**carry c1 (i1, i2, C);**

**endmodule**

**--------------------------------------------------**

**module Test; //test bench to test HA (Half Adder)**

**// Inputs**

**reg A, B;**

**// Outputs**

**wire Sum, Carry;**

**// Instantiate the Unit/Design Under Test (U/DUT)**

**HA dut (.i1(A), .i2(B), .S(Sum), .C(Carry));**

**initial begin**

**// Initialize Inputs**

**A = 1;**

**B = 1;**

**#100**

**A = 1;**

**B = 0;**

**#150**

**A = 0;**

**B = 1;**

**#150**

**A = 0;**

**B = 0;**

**end**

**endmodule**